

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0033] with the following amended paragraph:

[0033] The ISEF 210 is coupled to the processing element 220. The ISEF 210 includes programmable logic for enabling application-specific instructions (“instruction extensions”) to be stored and executed. The ISEF 210 provides the ability to add additional instructions to a set of standard instructions for the processing element 220. The ISEF 210 is a type of software extensible device. In some embodiments, the ISEF 210 comprises a programmable logic device. One example of the ISEF 210 is described in U.S. Application Serial Number 10/404,706 filed on March 31, 2003 and titled “Reconfigurable Instruction Set Computing Extension Adapter”, which is hereby incorporated by reference.

Please replace paragraph [0034] with the following amended paragraph:

[0034] The processing element 220 is a processor configured to execute applications. The processing element 220 includes a standard or native instruction set that provides a set of instructions that the processor element 220 is designed to recognize and execute. These standard instructions are hard-coded into the silicon and cannot be modified. One example of the processing element 220 is an Xtensa processor, from Tensilica, Inc., of Santa Clara, California. One example of the processing element 220 is also described in U.S. Application Serial Number 10/404,706 filed on March 31, 2003 and titled “Reconfigurable Instruction Set Computing Extension Adapter.”

Please replace paragraph [0045] with the following amended paragraph:

[0045] The data cache 323 and the instruction cache 324 are used, for example, to contain data and instructions, respectively, that the processing element 322 requires to perform its dedicated functionality. These local caches allow data and instructions to be readily accessible to optimize the processing performance. The ISEF 321 can be extensible and customizable such that it can be configured by way of programmable logic to implement new instructions for execution. The new instructions and the ISEF 321 are described in the technology incorporated by reference, such as those described in the U.S. Patent Application entitled "System and Method for Efficiently Mapping Heterogeneous Objects Onto an Array of Heterogeneous Programmable Logic Resources," U.S. Application Ser. No. 10/404,680 filed March 31, 2003, now U.S. Patent No. 7,000,211 under Attorney Docket No. PA2586, which is hereby incorporated by reference.